REMARKS

An excess claim fee payment letter is attached hereto to cover the cost of any excess claims.

Claims 29-39 and 41-54 are all the claims presently pending in the application. Claims 29, 32, 36, 41 and 45-46 have been amended to more particularly define the invention. Claims 50-54 have been added to claim additional features of the invention. Attached hereto is a marked-up version of the changes made to the specification and claims by the current Amendment.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and <u>not</u> for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 29, 34-36, 41-42 and 45-46 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ohata et al. (U.S. Patent No. 4,837,186). Claims 30, 32-33 and 47-49 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ohata et al. (U.S. Patent No. 4,837,186), or alternatively under 35 U.S.C. § 103(a) as being unpatentable over Ohata. Claim 31 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohata et al. (U.S. Patent No. 4,837,186). Claims 37-39 and 43-44 stand rejected under 35 U.S.C. § 103(a) as bing unpatentable over Ohata et al. in view of Tanaka (JP-10-303385).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor device (e.g., a hybrid semiconductor substrate) having a bulk silicon region including single crystal silicon, and a silicon-on-insulator (SOI) region. The SOI region includes an insulator layer which is formed beneath an upper portion of the single crystal silicon and has at least one lateral end portion adjacent to a lower portion of the single crystal silicon, and at least one isolation oxide formed in the upper portion of the single crystal silicon so as to form at least one island of

single crystal silicon on an upper surface of the insulator layer. Importantly, the upper portion of the single crystal silicon and the lower portion of said single crystal silicon have a same crystal orientation.

Conventional substrates having an SOI region are formed either by separation by implantation of oxygen (SIMOX) or by a cladding process where an oxide layer is formed in a first surface of a first substrate, a second substrate is bonded to the first surface, and elements are then formed in the second substrate. However, neither of these processes can form a semiconductor device in which the upper portion of the single crystal silicon (e.g., a portion above the insulator layer) and the lower portion of said single crystal silicon have a same crystal orientation.

The claimed semiconductor device, on the other hand, may include single crystal silicon in which the upper portion of the single crystal silicon and the lower portion of said single crystal silicon have a same crystal orientation. Specifically, the upper portion of single crystal silicon may be formed over the insulator layer by depositing amorphous silicon on the insulator layer and the lower portion of the single crystal silicon, and then crystallizing (e.g., by annealing) the amorphous silicon by using the lower portion of said single crystal silicon as a crystal growth seed. Thus, the claimed device has a higher substrate quality than conventional devices.

II. THE PRIOR ART REFERENCES

A. The Ohata Reference

The Examiner alleges that Ohata anticipates the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Ohata.

Ohata discloses a silicon semiconductor substrate with an insulating layer therein. The silicon semiconductor substrate comprises a first silicon plate, an insulating layer embedded in the first silicon plate so that the surfaces of the silicon plate and the insulating layer are in a mirror surface, and a second silicon plate united with the first silicon plate and the insulating layer at the mirror surface of the first silicon plate and the insulating layer

(Ohata at Abstract)

However, contrary to the Examiner's allegations, Ohata does not teach or suggest "wherein said upper portion of said single crystal silicon and said lower portion of said single crystal silicon have a same crystal orientation" as recited in claim 29 and similarly recited in claims 41 and 45-46. As noted above, conventional substrates having an SOI region are formed either by separation by implantation of oxygen (SIMOX) (Application at page 5, lines 2-10) or by a cladding process where an oxide layer is formed in a first surface of a first substrate, a second substrate is bonded to the first surface, and elements are then formed in the second substrate. However, neither of these processes can form a semiconductor device in which the upper portion of the single crystal silicon (e.g., a portion above the insulator layer) and the lower portion of said single crystal silicon have a same crystal orientation.

The claimed semiconductor device, on the other hand, may include single crystal silicon in which the upper portion of the single crystal silicon and the lower portion of said single crystal silicon have a same crystal orientation (Application at Figure 1D; page 9, lines 18-22). Specifically, the upper portion of single crystal silicon may be formed over the insulator layer by depositing amorphous silicon on the insulator layer and the lower portion of the single crystal silicon, and then growing (e.g., depositing) the single crystal silicon over the insulator layer and then crystallizing (e.g., by annealing) the amorphous silicon by using the lower portion of said single crystal silicon as a crystal growth seed. (Application at page 3, line 18-page 4, line 12; page 9, lines 12-22). Thus, the claimed device has a higher substrate quality than conventional devices (Application at page 5, lines 2-10).

Clearly, Ohata does not teach or suggest these novel features. Indeed, the device in Ohata is formed by a completely different process than the claimed device, and results in a completely different structure than the claimed device. In fact, the Ohata device has a structure which is very similar to the conventional devices discussed in the background section of the Application (Application at page 5, lines 2-10). Thus, the claimed device is likely to have a substrate which has fewer defects than the Ohata device.

The Examiner apparently equates the first silicon plate 21 and second silicon plate 22 in Ohata with the single crystal silicon of the claimed device. Specifically, the Examiner

states that "the single crystal silicon over the insulator layer has the same crystal orientation and structure as that in the bulk silicon region, because it is the same silicon crystal silicon layer". However, Applicant respectfully submits that the Examiner is clearly misreading Ohata. Indeed, nowhere does Ohata disclose that the layers 21 and 22 in Ohata are "the same silicon crystal layer". Indeed, Ohata clearly discloses that these layers are two separate layers (e.g., a first monocrystalline plate 21 and a second N-monocrystalline plate 22), not one layer, as alleged by the Examiner. Moreover, it is clear that these layers 21 and 22 have to be two separate and unrelated layers based on the process that Ohata uses to form the device.

Specifically, referring to Figures 6A-6D, Ohata explains that in his process an SiO_2 layer 23a is formed in the first monocrystalline plate 21, and then the second N-monocrystalline plate 22 merely "comes into contact" with the first plate 21 (Ohata at col. 4, lines 39-41). Then the first plate 21 and second plate 22 are subjected to heat treatment "so that the first and second silicon plates 21 and 22 are rigidly united".

This is absolutely all that Ohata discloses about these two plates. In other words, there is absolutely no relationship between them disclosed. Certainly, there is no teaching or suggestion of any similarity in crystal orientation or structure between these two plates (Applicant notes that the heat treatment in Ohata is merely to facilitate a bond between the two plates and not to affect the crystalline structure of the plates). Therefore, the Examiner has absolutely no reason to suggest that there is such a similarity other than relying upon impermissible hindsight.

Therefore, Applicant submits that Ohata does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Tanaka Reference

The Examiner alleges that Tanaka would have been combined with Ohata to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Tanaka discloses a method of forming a hybrid element on a SIMOX wafer. Specifically, a silicon substrate 3 is exposed by selectively removing a silicon layer 1 and an insulating layer 2 from a silicon-on-insulator (SOI) substrate. The desired semiconductor elements 11 are respectively formed on the exposed silicon substrate 3 and the silicon layer 1 (Tanaka at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters and different problems. Specifically, Ohata is merely directed to a method of forming an insulating layer in a substrate, whereas Tanaka is directed to a well-known SIMOX process for forming a logic circuit and memory cell on a substrate. Clearly, these references teach away from each other and would not have been combined by one of ordinary skill in the art.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that "[i]t would have been obvious ... to form a DRAM memory device on the silicon bulk and a MOSFET logic device on the SOI region, as taught by Tanaka, in Ohata et al.'s device in order to provide a hybrid device wherein the DRAM can operate at high speed with less power consumption and the logic circuits are adequately isolated" which is merely a conclusory statement and insufficient to support the combination of these disparate references.

Moreover, Tanaka, like Ohata, does not teach or suggest "wherein said upper portion of said single crystal silicon and said lower portion of said single crystal silicon have a same crystal orientation" as recited in claim 29 and similarly recited in claims 41 and 45-46. As noted above, unlike conventional devices which are formed by SIMOX processes, the claimed semiconductor device may include single crystal silicon in which the upper portion of the single crystal silicon and the lower portion of said single crystal silicon have a same crystal orientation (Application at Figure 1D; page 9, lines 18-22).

Specifically, in the claimed device, the upper portion of single crystal silicon may be formed over the insulator layer by depositing amorphous silicon on the insulator layer and the lower portion of the single crystal silicon, and then crystallizing (e.g., by annealing) the

amorphous silicon by using the lower portion of said single crystal silicon as a crystal growth seed. (Application at page 3, line 18-page 4, line 12; page 9, lines 12-22). Thus, the claimed device has a higher substrate quality than conventional devices (Application at page 5, lines 2-10).

Clearly, Tanaka does not teach or suggest these novel features. Indeed, Tanaka merely describes a device in which portions of a silicon layer 1 and insulating layer 2 are selectively removed, and elements formed in the exposed surfaces. In other words, nowhere does Tanaka disclose a device with single crystal silicon with an upper portion (e.g., over an insulator layer) and a lower portion have a same crystal orientation.

In addition, as noted above, the Tanaka device is formed by a conventional SIMOX process, which results in an unacceptable substrate. For instance, in the Background section o the Application, it is explained that "as compared to the conventional patterned SIMOX technique, which results in a much higher number of defect counts per unit area (or defect density), the method of the present invention results in a much better substrate quality" (Application at page 5, lines 3-6).

In other words, Tanaka does not teach or suggest a method of producing a substrate that can result in the structure of the claimed invention. For example, Tanaka does not teach or suggest depositing amorphous silicon on an insulator layer and a lower portion of single crystal silicon, and then crystallizing (e.g., by annealing) the amorphous silicon by using the lower portion of said single crystal silicon as a crystal growth seed.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

Applicant notes that the claims as stated on pages 1-4 of the Amendment filed herein on March 4, 2002 may have contained some inconsistencies with the correct version of the claims on pages 14-16 of that Amendment. Therefore, to clarify the state of the claims,

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Applicant has included in this Amendment a correct copy of all of the claims 29-39 and 41-49, even if the some of the claims were unamended by this Amendment.

In view of the foregoing, Applicant submits that claims 29-39 and 41-54, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 10/31/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims to read as follows:

29. (Thrice Amended) A semiconductor device comprising:

a bulk silicon region comprising single crystal silicon; and

a silicon-on-insulator (SOI) region comprising:

an insulator layer which is formed beneath an upper portion of said single crystal silicon and has at least one lateral end portion adjacent to a lower portion of said single crystal silicon; and

at least one isolation oxide formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer,

<u>wherein said upper portion of said single crystal silicon and said lower portion of said single crystal silicon have a same crystal orientation</u>

[wherein a sidewall of said insulator layer is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer].

32. (Amended) The semiconductor device according to claim 29, wherein said upper portion of said single crystal silicon is formed over said insulator layer by depositing amorphous silicon on said insulator layer and said lower portion of said single crystal silicon, and <u>crystallizing said amorphous silicon by</u> [horizontally growing said single crystal silicon over said insulator layer] using said lower portion of said single crystal silicon as a crystal growth seed.

36. (Twice Amended) The semiconductor device according to claim 29, <u>wherein a sidewall of said insulator layer is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer</u> [wherein said single crystal silicon over said insulator layer has a same crystal orientation and structure as said single crystal silicon in said bulk silicon region].

41. (Four Times Amended) A hybrid bulk silicon and silicon-on-insulator (SOI) substrate, comprising:

an insulator layer which is formed beneath an upper portion of single crystal silicon and has at least one lateral end portion adjacent a lower portion of said single crystal silicon; and

a plurality of isolation oxides formed in said upper portion of said single crystal silicon so as to form at least one island of said single crystal silicon on an upper surface of said insulator layer,

<u>wherein said upper portion of said single crystal silicon and said lower portion of said single crystal silicon have a same crystal orientation</u> [wherein a sidewall of said insulator layer is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer].

45. (Four Times Amended) A semiconductor device comprising:

a bulk semiconductor region comprising semiconductor substrate; and

a semiconductor-on-insulator region comprising:

an insulator layer which is formed beneath an upper portion of said semiconductor substrate and has at least one lateral end portion adjacent to a lower portion of said semiconductor substrate; and

at least one isolation oxide formed in said upper portion of said semiconductor substrate so as to form at least one island of said semiconductor substrate on an upper surface of said insulator layer,

<u>wherein said upper portion of said semiconductor substrate and said lower portion of said semiconductor substrate have a same crystal orientation</u> [wherein a sidewall of said insulator layer is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer].

46. (Thrice Amended) A semiconductor device comprising:

a single crystal silicon substrate having a lower portion and an upper portion;

an insulator layer which is formed beneath said upper portion of said single crystal silicon substrate and has at least one lateral end portion adjacent to said lower portion of said single crystal silicon substrate; and

at least one isolation oxide formed in said upper portion of said single crystal silicon substrate so as to form at least one island of said single crystal silicon substrate on an upper surface of said insulator layer,

<u>wherein said upper portion of said single crystal silicon substrate and said lower portion of said single crystal silicon substrate have a same crystal orientation</u> [wherein a sidewall of said insulator layer is angled so that a width of said upper surface of said insulator layer is larger than a width of a lower surface of said insulator layer].